

Fig. 1

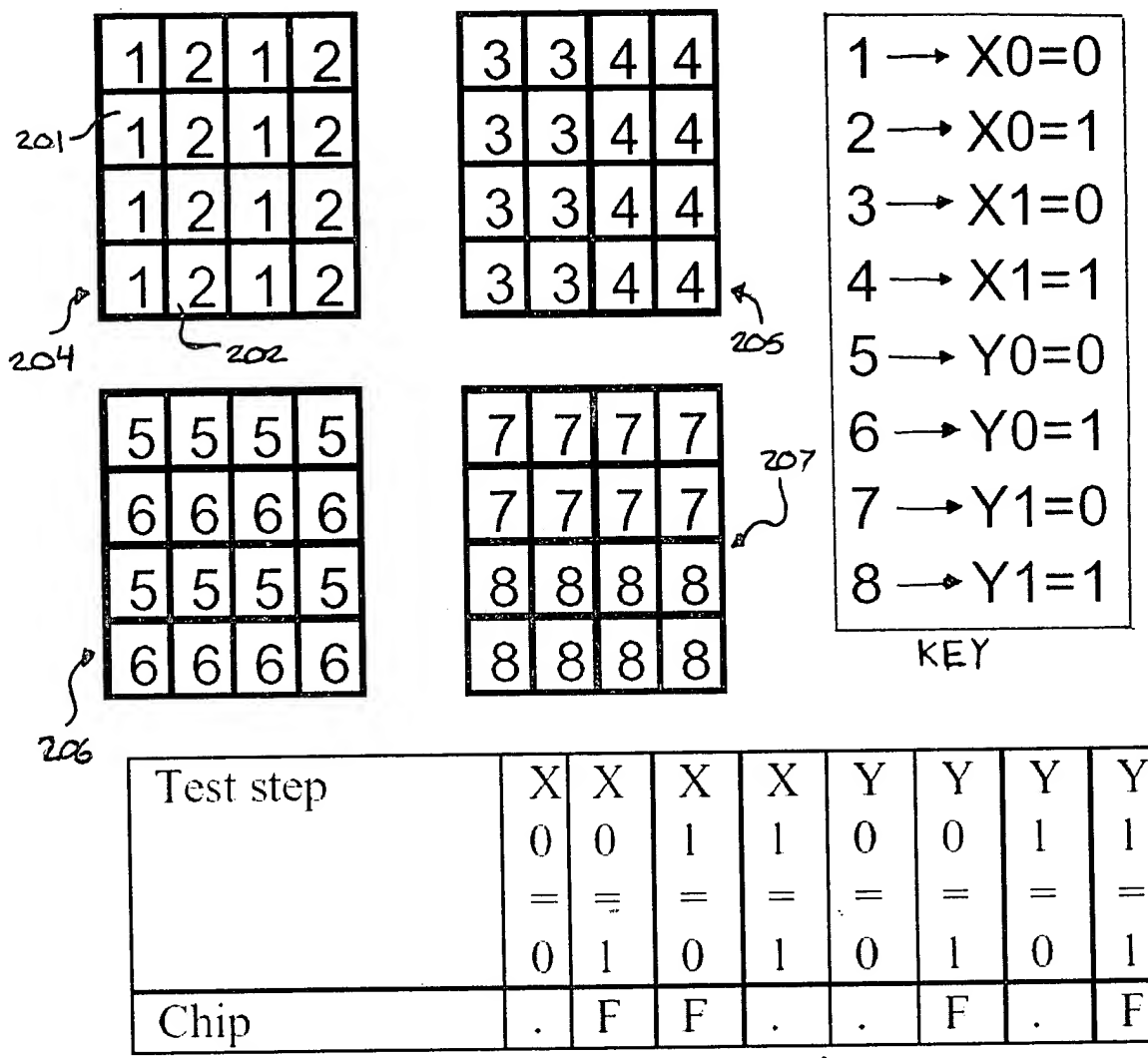


Fig. 2

200

109T80" 52TTE660

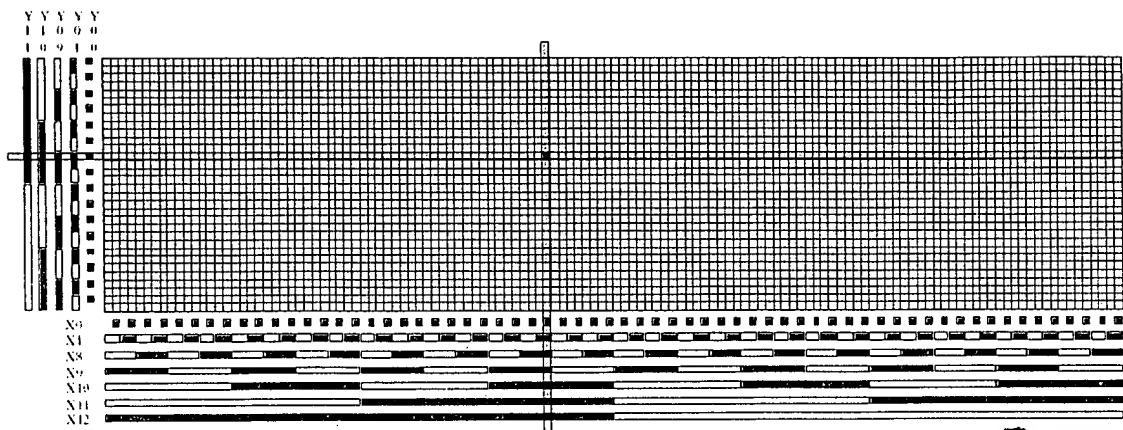


Fig. 3a

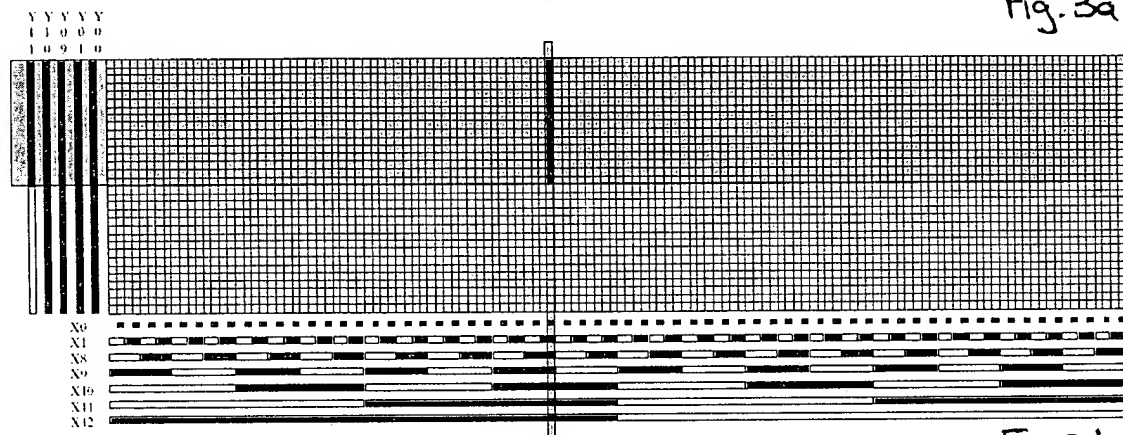


Fig. 3b

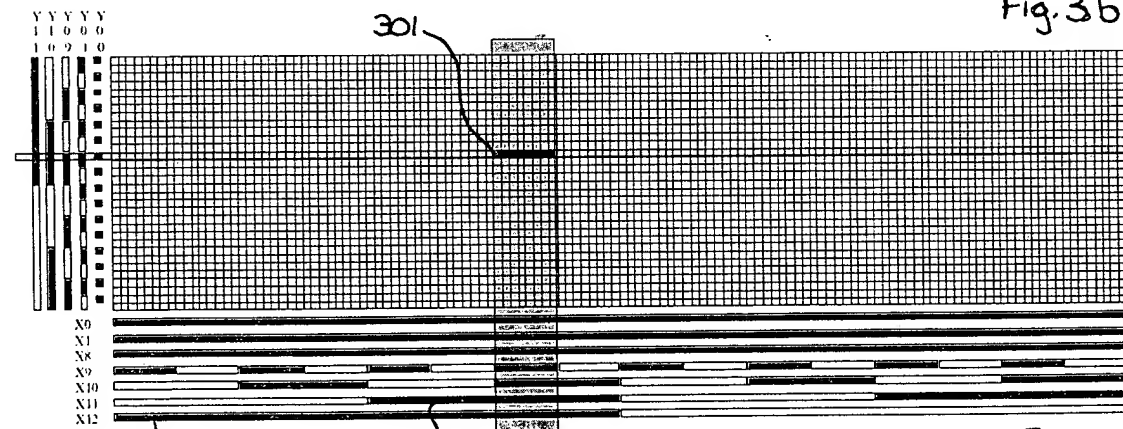


Fig. 3c

1	2	1	2
3	4	3	4
1	2	1	2
3	4	3	4

5	5	6	6
5	5	6	6
7	7	8	8
7	7	8	8

1 $x_0=0, y_0=0$

2 $x_0=1, y_0=0$

3 $x_0=0, y_0=1$

4 $x_0=1, y_0=1$

5 $x_1=0, y_1=0$

6 $x_1=0, y_1=1$

7 $x_1=1, y_1=0$

8 $x_1=1, y_1=1$

Fig. 4

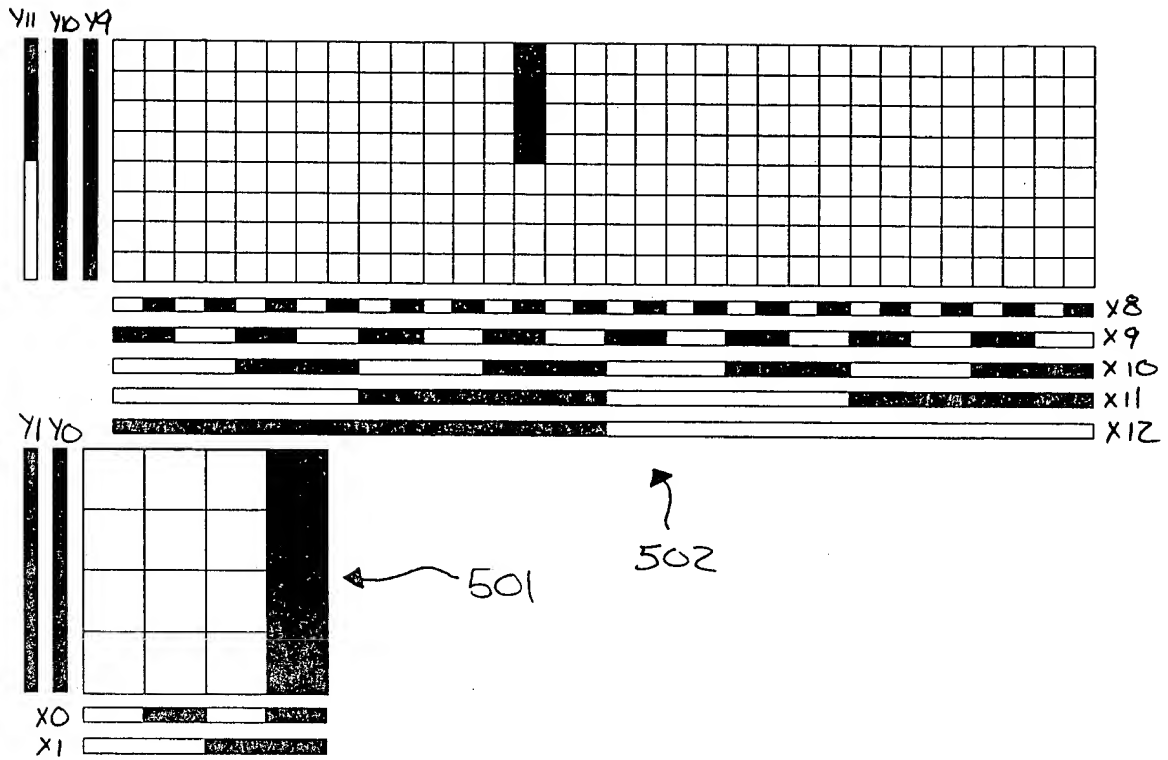


Fig. 5

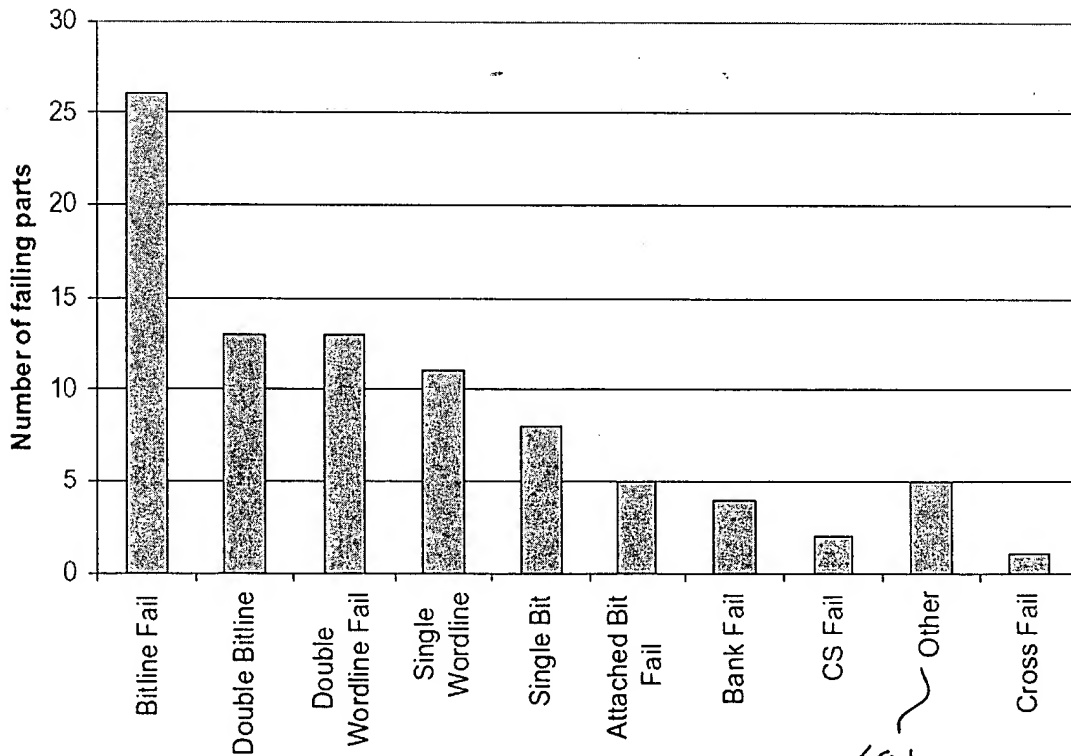
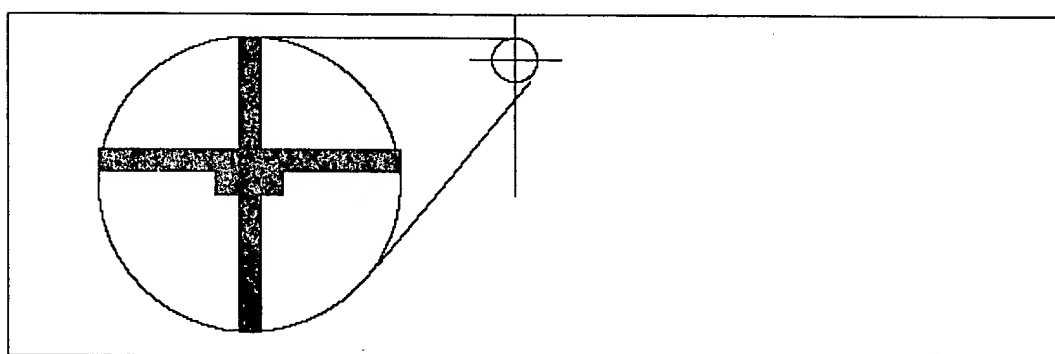
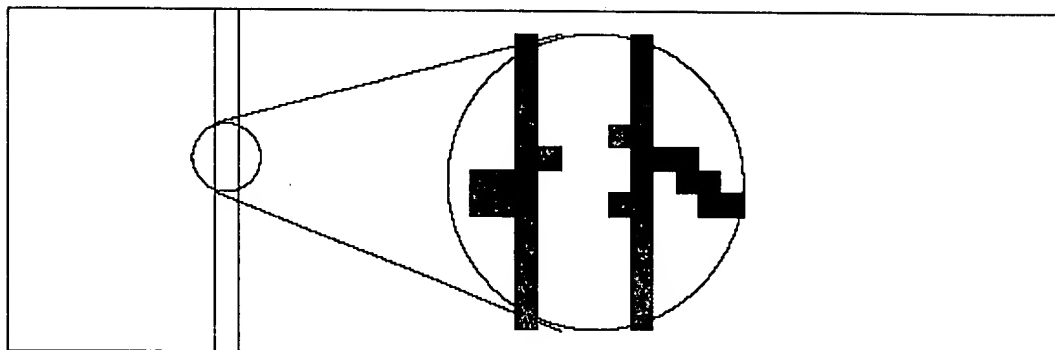


Fig. 6

256k SRAM 139 145



246

Fig. 7

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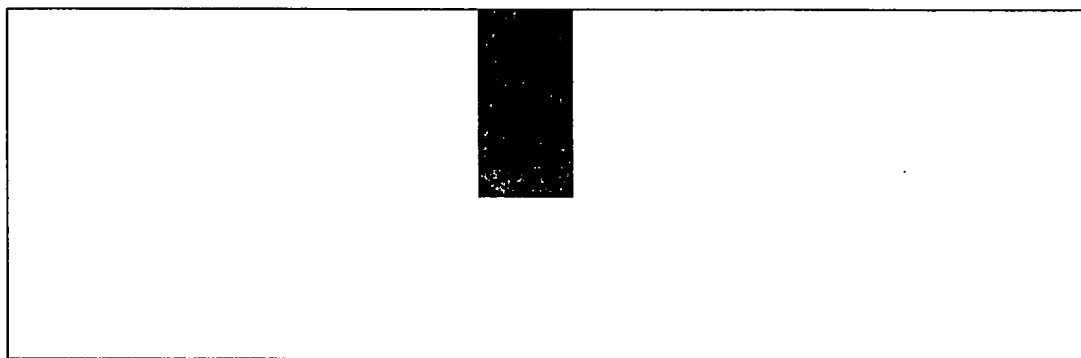
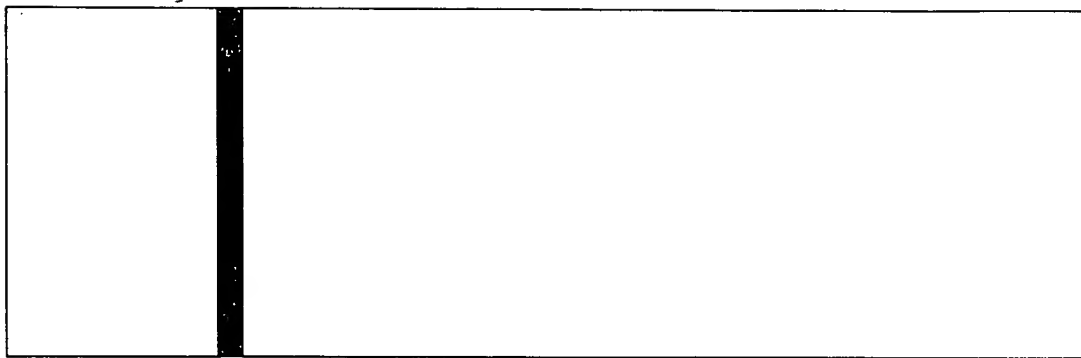


Fig. 8

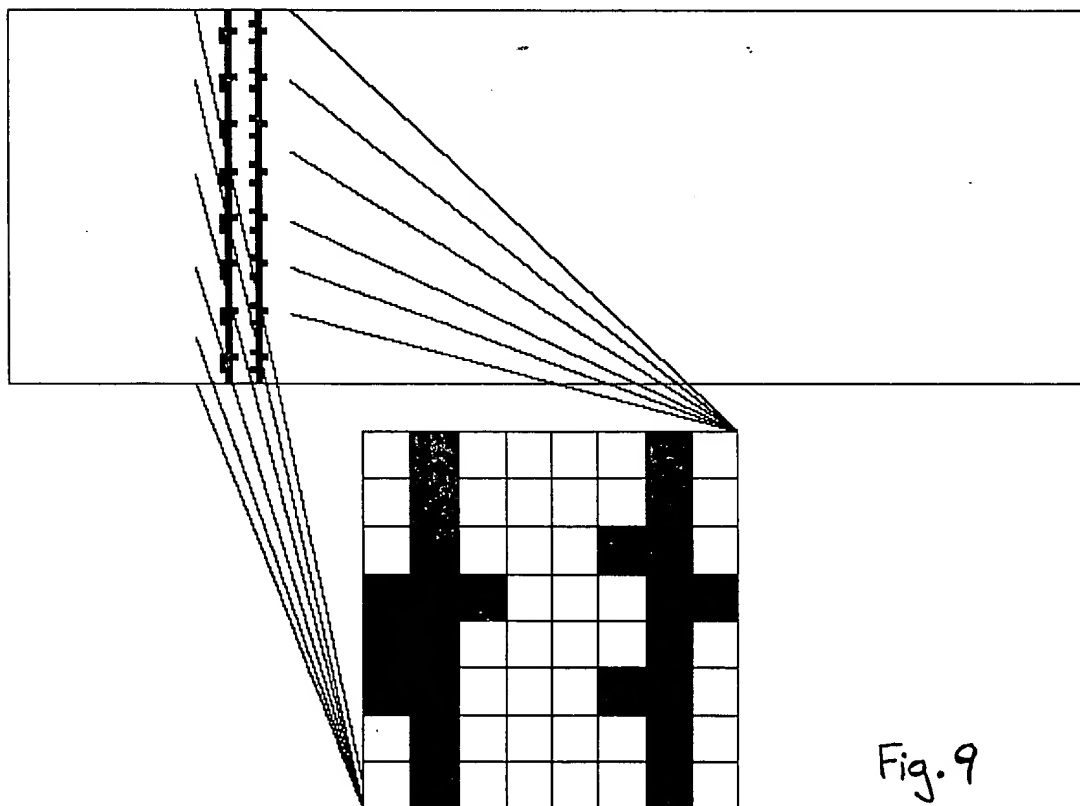


Fig. 9

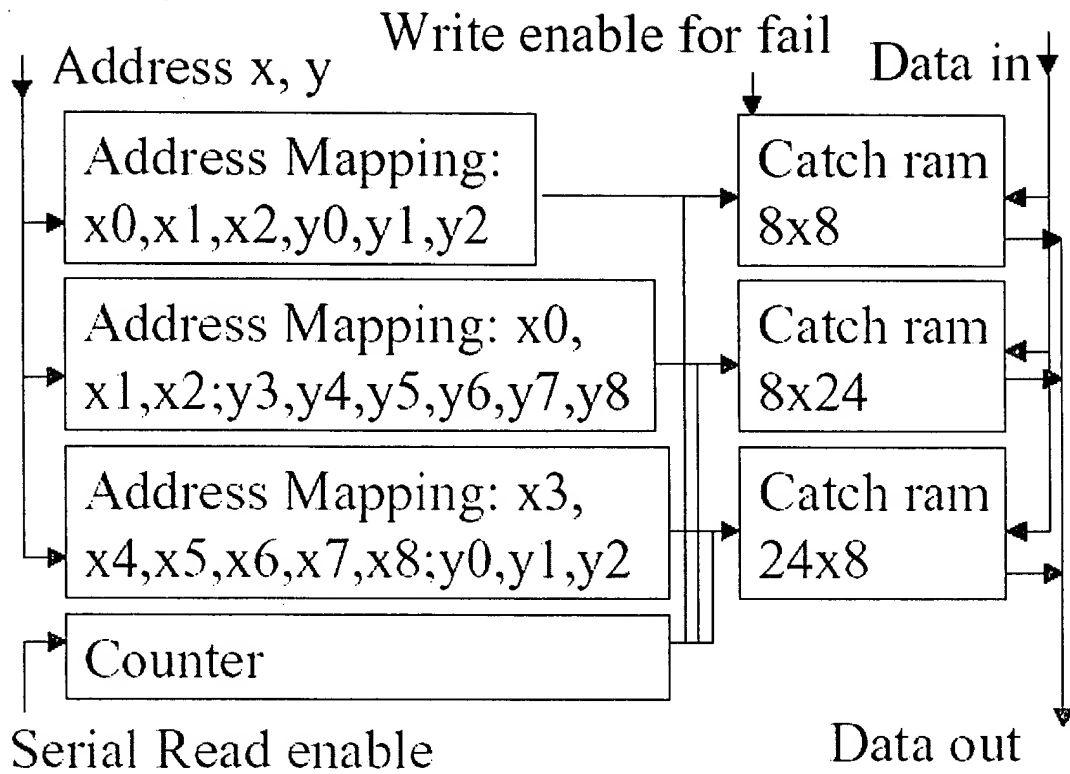


Fig. 10

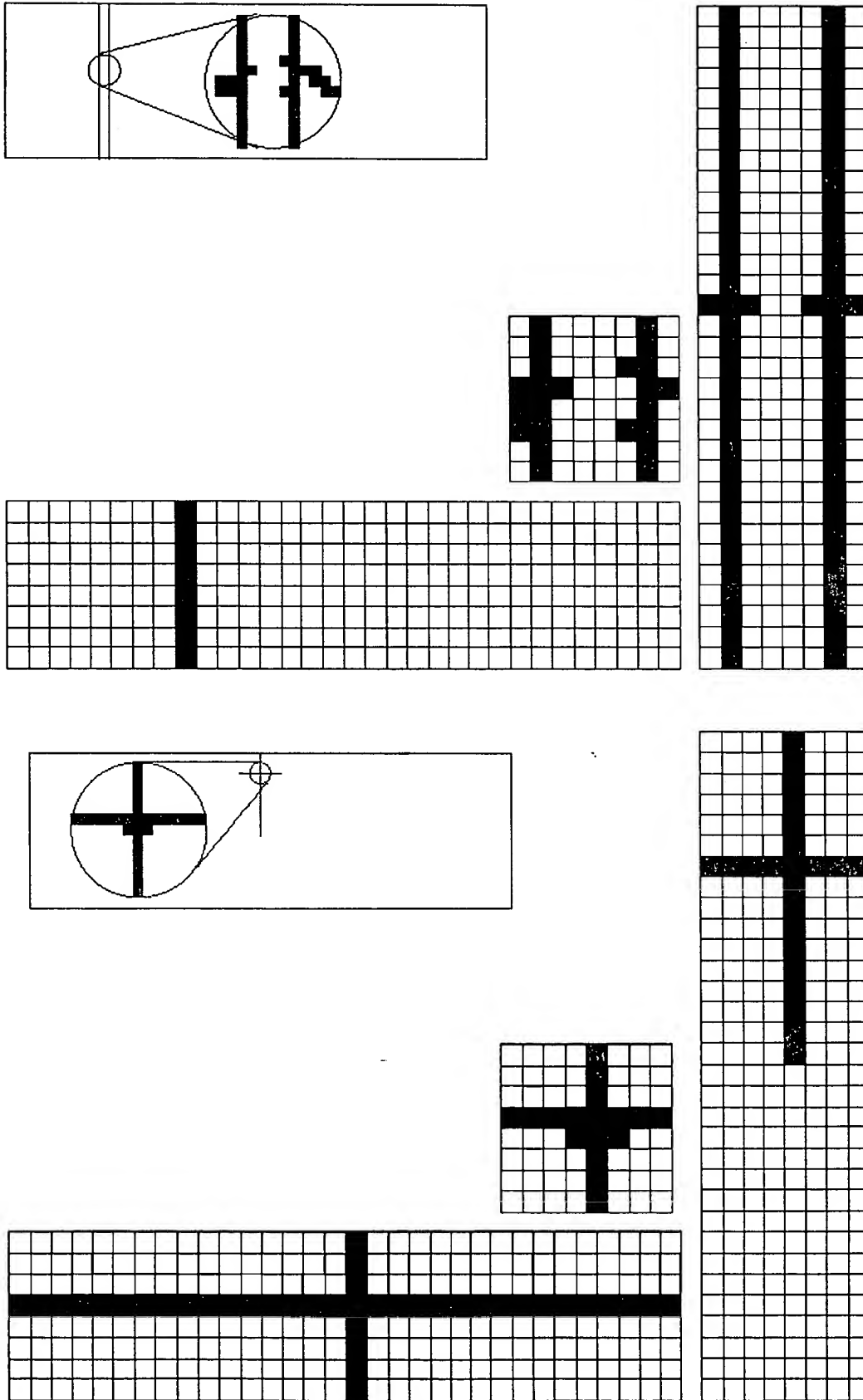


Fig. 11

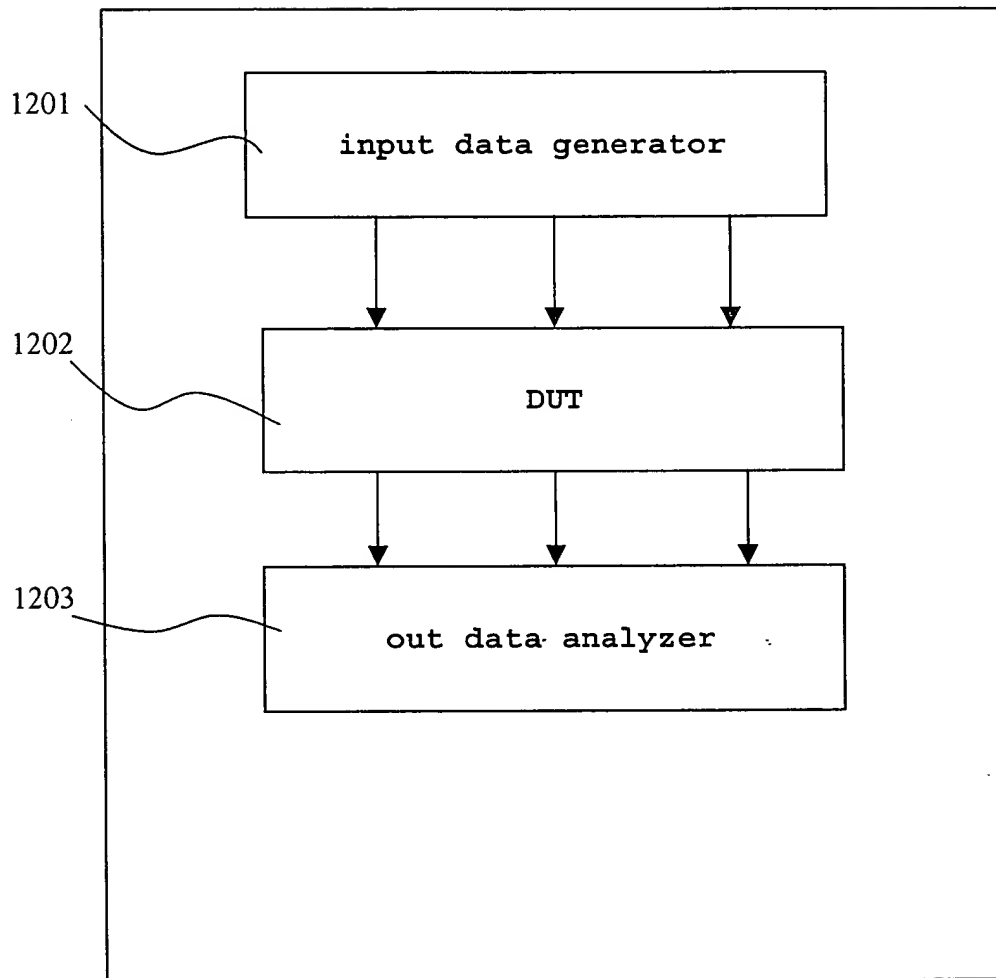


Fig. 12

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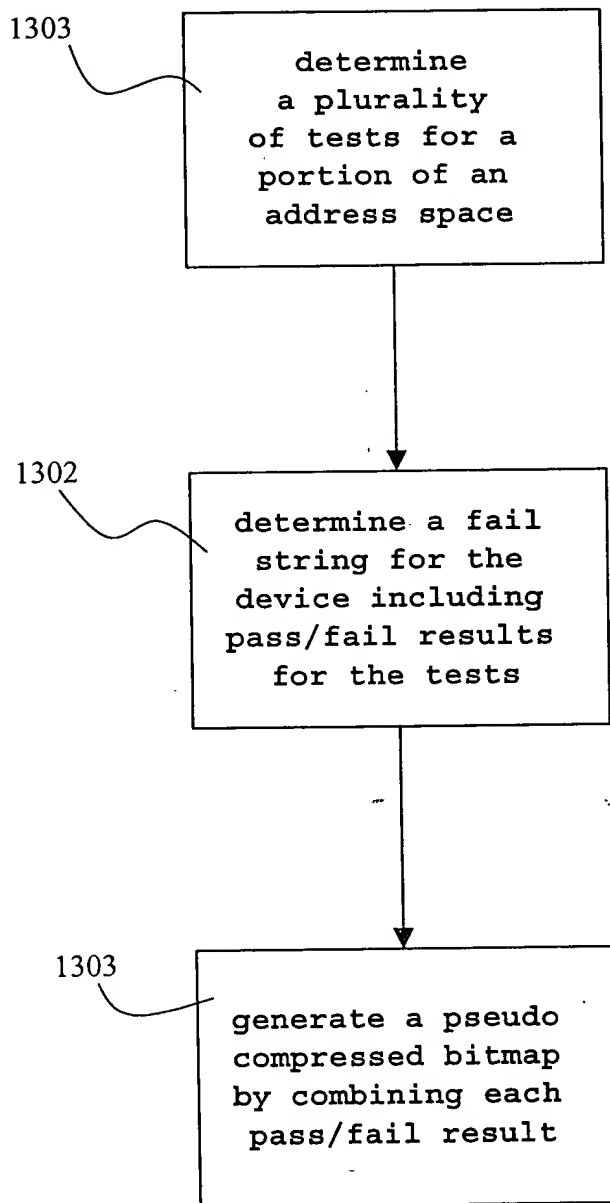


Fig. 13